



**SPECIFICATIONS
FOR LCD MODULE**

MATRIX ORBITAL NO.	MOP-GL12232D
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DOCUMENT REVISION HISTORY:

DATE	PAGE	DESCRIPTION
2000.8.	-	First release
2005.3.	-	Modify the full specification
2005.12.	-	Update the part number system

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1. Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

2. General Specification

Item	Dimension	Unit
Number of Dots	122 x 32	□
Module dimension(With LED Backlight)	65.8 x 27.0 x 12.0□MAX□	mm
View area	60.2 x 18.0	mm
Active area	53.64 x 14.04	mm
Dot size	0.40 x 0.40	mm
Dot pitch	0.44 x 0.44	mm
LCD type	STN	
Duty	1/32	
View direction	6 o'clock or 12 o'clock	
Backlight Type	WHITE BACKLIGHT	

3. Absolute Maximum Ratings

Item		Symbol	Min	Max	Unit
Input Voltage		V_I	-0.3	VDD+0.3	V
Supply Voltage For Logic		VDD-V _{SS}	-0.3	7.0	V
Supply Voltage For LCD		V _{DD} -V ₀	Vdd-13.5	0	V
Standard	Operating Temp.	Top	0	50	□
Temperature LCM	Storage Temp.	Tstr	-10	60	□
Wide Temperature	Operating Temp.	Top	-20	70	□
LCM	Storage Temp.	Tstr	-30	80	□

4. Electrical Characteristics

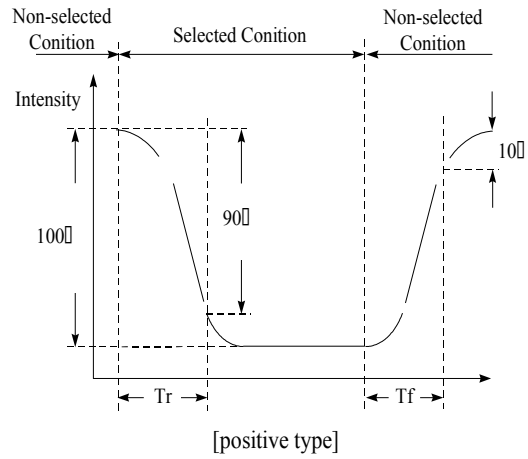
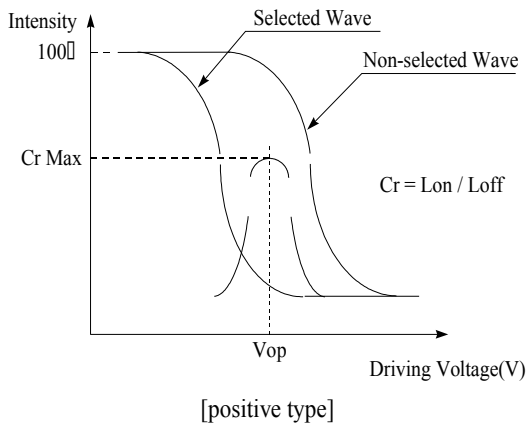
Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V _{DD} -V _{SS}	□	4.5	5.0	5.5	V
Supply Voltage For LCD	V _{DD} -V ₀	Ta=25□	-	4.8	-	V
Input High Volt.	V _{IH}	□	0.7 V _{DD}	□	V _{DD}	V
Input Low Volt.	V _{IL}	□	V _{SS}	□	0.3 V _{DD}	V
Supply Current	I _{DD}	V _{DD} =5V	-	1.0	2.0	mA
Supply Voltage of backlight	V _{LED}	Forward current =20 mA	-	3.6	-	V

5. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ	CR \geq 2	-20	\square	35	deg
	(H) ϕ	CR \geq 2	-30	\square	30	deg
Contrast Ratio	CR	\square	\square	3	\square	\square
Response Time	T rise	\square	\square	\square	250	ms
	T fall	\square	\square	\square	250	ms

Definition of Operation Voltage (Vop)

Definition of Response Time (Tr, Tf)



Conditions :

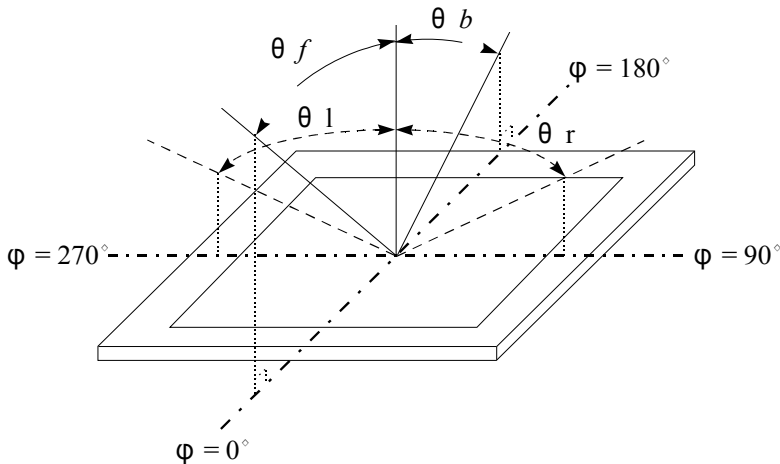
Operating Voltage : Vop

Viewing Angle(θ / ϕ) : $0^\circ \sim 0^\circ$

Frame Frequency : 64 HZ

Driving Waveform : 1/N duty , 1/a bias

Definition of viewing angle(CR \geq 2)

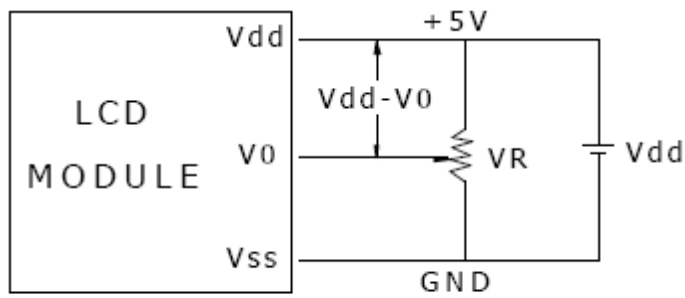


6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	RS	H/L	Register Select
2	E2	H/L	Enable For Chip2, Active High, Left Part
3	E1	H/L	Enable For Chip1, Active High, Left Part
4,5	NC	NC	NC
6	RW	H/L	Read/Write
7	V _{SS}	0V	Ground
8	DB0	H/L	Data bit 0
9	DB1	H/L	Data bit 1
10	DB2	H/L	Data bit 2
11	DB3	H/L	Data bit 3
12	DB4	H/L	Data bit 4
13	DB5	H/L	Data bit 5
14	DB6	H/L	Data bit 6
15	DB7	H/L	Data bit 7
16	V _{DD}	5.0V	Supply Voltage for logic
17	RSE	H/L	Reset Signal
18	V0		Operating voltage for LCD
19	NC	NC	NC
20	NC	NC	NC

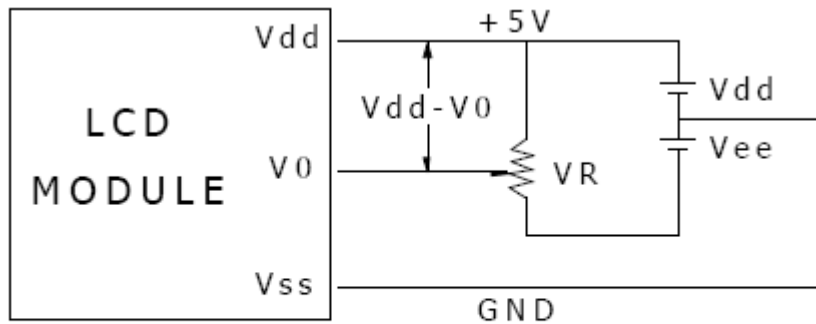
7. POWER SUPPLY

SINGLE SUPPLY VOLTAGE TYPE (for LCM with Negative Power on PCB)



Vdd-V0: LCD Driving Voltage
VR: 10K - 20K

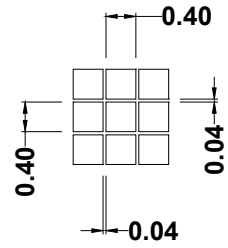
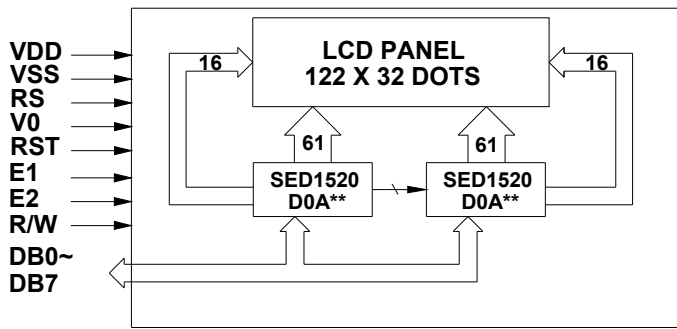
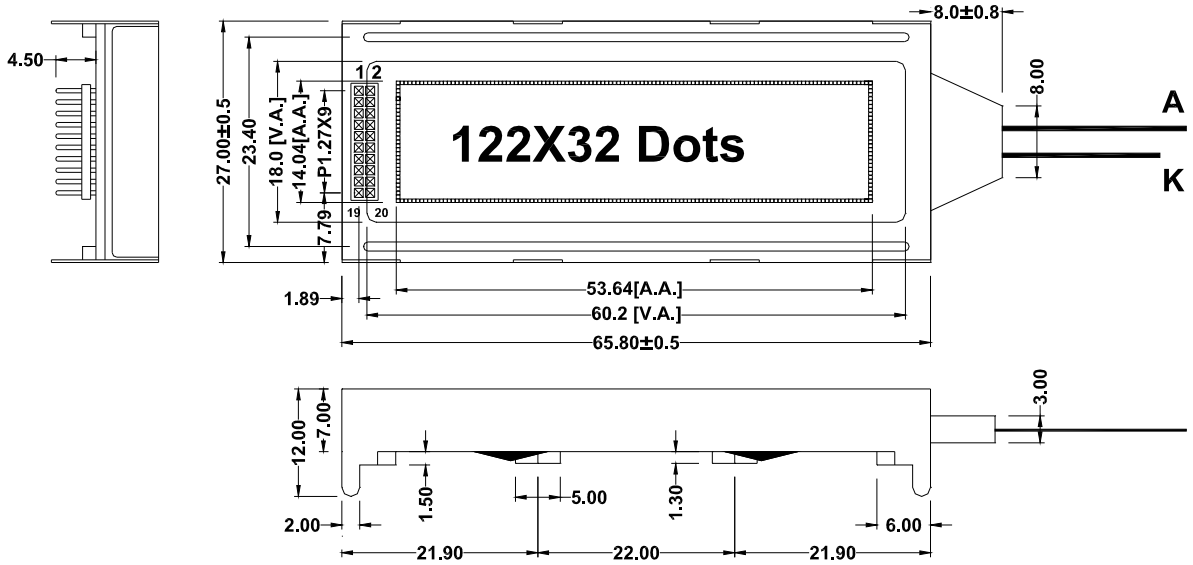
DUAL SUPPLY VOLTAGE TYPE (for LCM without Negative Power on PCB)



Vdd-V0: LCD Driving Voltage
VR: 10K - 20K

8. Contour Drawing & Block Diagram

LED B/L



**** OR EQUIVALENT**

9. Timing Characteristics

● AC Characteristics

○ Read/Write timing for the 80-port MPU

($T_a = -20$ to 75°C , $V_{SS} = -5.0\text{V} \pm 10\%$)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
Address hold time	A0, $\overline{\text{CS}}$	t_{AHB}		10	—	—	ns
Address set-up time		t_{AWB}		20	—	—	ns
System cycle time	$\overline{\text{WR}}$, $\overline{\text{RD}}$	t_{CYC8}		1000	—	—	ns
Control pulse width		t_{CC}		200	—	—	ns
Data set-up time	D0 ~ D7	t_{DS8}	$C_L = 100\text{pF}$	80	—	—	ns
Data hold time		t_{DH8}		10	—	—	ns
$\overline{\text{RD}}$ access time		t_{ACC8}		—	—	90	ns
Output disable time		t_{OH8}		10	—	60	ns

*2. The ratings when $V_{SS} = -3.0\text{V}$ are approximately 100% higher than when $V_{SS} = -5.0\text{V}$.

○ Read/Write timing for the 68-port MPU

($T_a = -20$ to 75°C , $V_{SS} = -5.0\text{V} \pm 10\%$)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
System cycle time	A0, $\overline{\text{CS}}$ R/ $\overline{\text{W}}$	t_{CYC6}^*3		1000	—	—	ns
Address set-up time		t_{AW6}		20	—	—	ns
Address hold time		t_{AH6}		10	—	—	ns
Data set-up time	D0 ~ D7	t_{DS6}	$C_L = 100\text{pF}$	80	—	—	ns
Data hold time		t_{DH6}		10	—	—	ns
Output disable time		t_{OH6}		10	—	60	ns
Access time		t_{ACC6}		—	—	90	ns
Enable pulse width	READ	E		100	—	—	ns
	WRITE			80	—	—	ns

*3. t_{CYC6} indicates the cycle during which $\overline{\text{CS}}/\overline{\text{E}}$ are HIGH; it does not indicate the cycle of the E signal.

*4. The ratings when $V_{SS} = -3.0\text{V}$ are approximately 100% higher than when $V_{SS} = -5.0\text{V}$.

○ Control timing for 80-port/68-port display

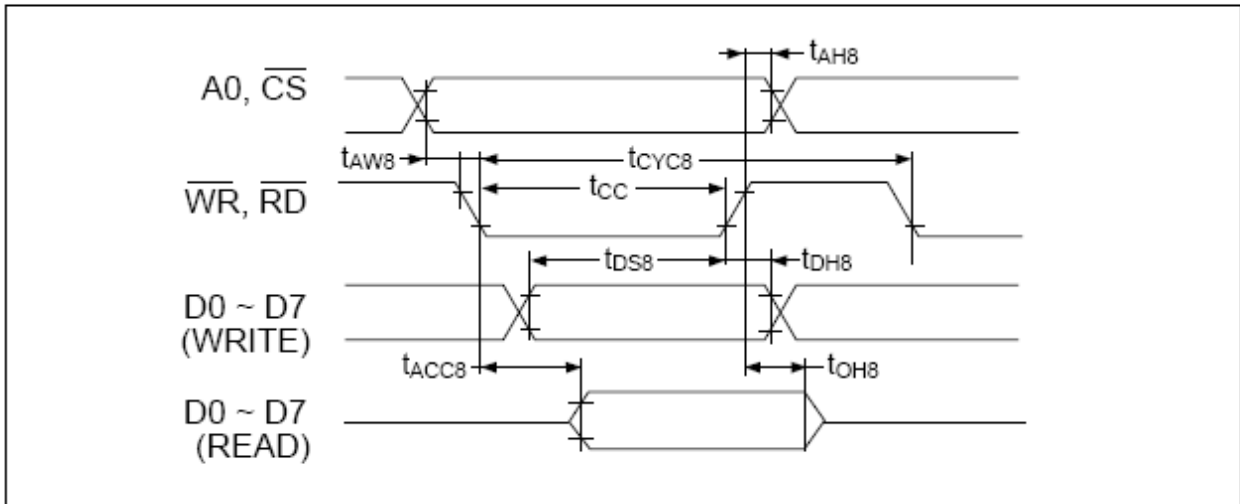
($T_a = -20$ to 75°C , $V_{SS} = -5.0\text{V} \pm 10\%$)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
LOW pulse width	CL	t_{WLCL}		35	—	—	μs
HIGH pulse width		t_{WHCL}		35	—	—	μs
Rising time		t_r		—	30	150	ns
Falling time		t_f		—	30	150	ns
FR delay time	FR	t_{DFR}	(Input timing)	-2.0	0.2	2.0	μs
			(Output timing), $C_L = 100\text{pF}$	—	0.2	0.4	

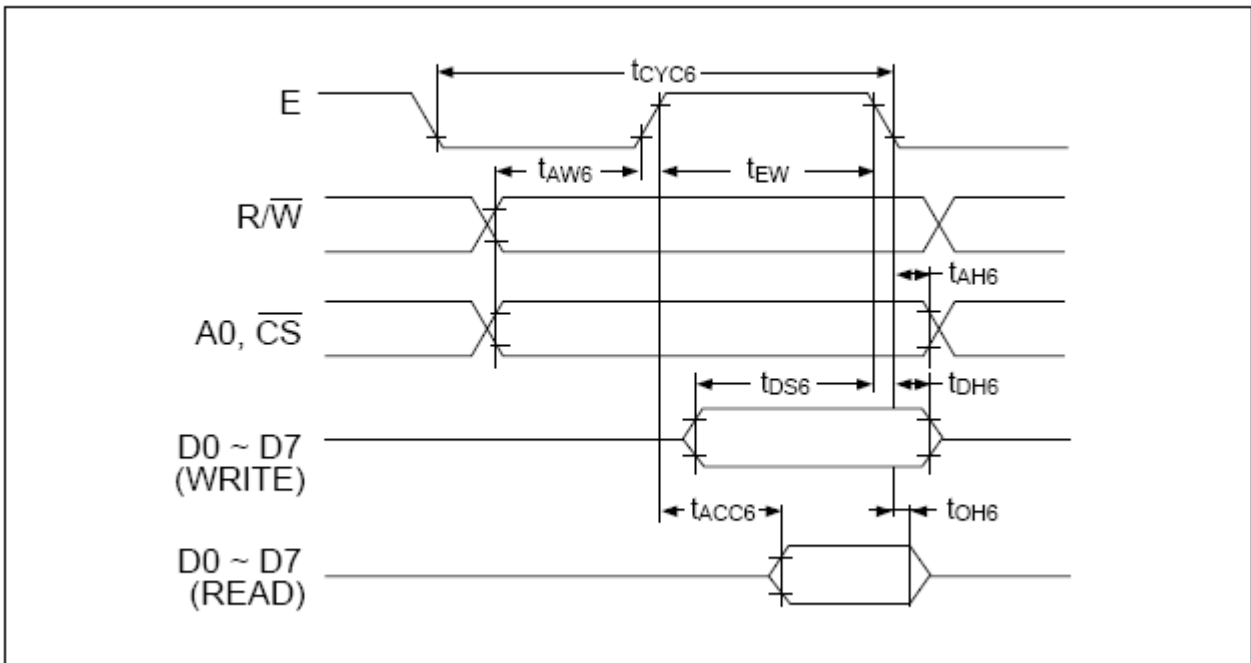
*5. The ratings when $V_{SS} = -3.0\text{V}$ are approximately 100% higher than when $V_{SS} = -5.0\text{V}$.

*6. The input timing of the FR delay time is determined by the SED1520 (Slave).
The output timing of the FR delay time is determined by the SED1520 (Master).

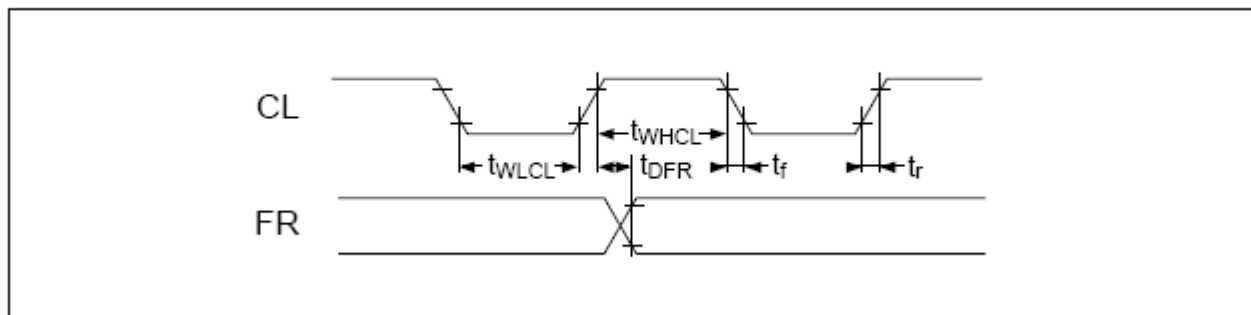
- Timing Chart
- Read/Write timing for the 80-port MPU



- Read/Write timing for the 68-port MPU



- Control timing for 80-port/68-port display



10. Instruction Table

■ DISPLAY COMMANDS

(Based on the 80-port MPU; the \overline{RD} and \overline{WR} commands differ for the 68-port MPU.)

Command	\overline{RD} \overline{WR} A0	D7 D6 D5 D4 D3 D2 D1 D0	Function
1 Display ON/OFF	1 0 0	1 0 1 0 1 1 1 0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. *7
2 Display START Line	1 0 0	1 1 0	Display START address (0~31) Determines the line of RAM data to be displayed at the display's top line (COM0).
3 Page Address Set	1 0 0	1 0 1 1 1 0	Page address (0~3) Sets the page of the Display RAM in the page address register.
4 Column (Segment) Address Set	1 0 0	0	Column address (0~79) Sets the column address of the Display RAM in the column address register.
5 Status Read	0 1 0	BUSY ACC ON/OFF RESET 0 0 0 0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ACC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6 Write Display Data	1 0 1	Write Data	Writes the data on the data bus to RAM
7 Read Display Data	0 1 1	Read Data	Reads data from the Display RAM onto the data bus.
8 ADC Select	1 0 0	1 0 1 0 0 0 0 0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9 Static Drive ON/OFF	1 0 0	1 0 1 0 0 1 0 0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *7 0: Normal display operation
10 Duty Select	1 0 0	1 0 1 0 1 0 0 0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty 0: 1/16 duty
11 Read Modify Write	1 0 0	1 1 1 0 0 0 0 0	Increments the column address counter by one only when display data is written but not when it is read.
12 End	1 0 0	1 1 1 0 1 1 1 0	Cancels the Ready Modify Write mode.
13 Reset	1 0 0	1 1 1 0 0 0 1 0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and page address register to 3.

*7. Power Save mode is entered by selecting static drive in Display OFF status.

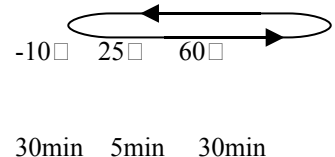
11.Quality Assurance

Screen Cosmetic Criteria

Item	Defect	Judgment Criterion	Partition
1	Spots	<p>A)Clear</p> <p><u>Size: d mm</u> <u>Acceptable Qty in active area</u></p> <p>d \leq 0.1 Disregard</p> <p>0.1 < d \leq 0.2 6</p> <p>0.2 < d \leq 0.3 2</p> <p>0.3 < d 0</p> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B)Unclear</p> <p><u>Size: d mm</u> <u>Acceptable Qty in active area</u></p> <p>d \leq 0.2 Disregard</p> <p>0.2 < d \leq 0.5 6</p> <p>0.5 < d \leq 0.7 2</p> <p>0.7 < d 0</p>	Minor
2	Bubbles in Polarizer	<p><u>Size: d mm</u> <u>Acceptable Qty in active area</u></p> <p>d \leq 0.3 Disregard</p> <p>0.3 < d \leq 1.0 3</p> <p>1.0 < d \leq 1.5 1</p> <p>1.5 < d 0</p>	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	<p>Not to be noticeable coloration in the viewing area of the LCD panels.</p> <p>Back-light type should be judged with back-light on state only.</p>	Minor

12. Reliability

Content of Reliability Test

Environmental Test			
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	60□ 96hrs	---
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-10□ 96hrs	---
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50□ 96hrs	---
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0□ 96hrs	---
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60□,90%RH 96hrs	---
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	50□,90%RH 96hrs	---
Temperature Cycle	Endurance test applying the low and high temperature cycle.  <p style="text-align: center;">-10□ 25□ 60□</p> <p style="text-align: center;">30min 5min 30min</p>	-10□/60□ 10 cycles	---

	1 cycle		
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msdc 3 times of each direction	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25□